ABSTRACT

A programmable logic integrated circuit has an embedded processor with a watchdog timer circuit. The watchdog timer circuit is used to detect software or hardware failures. In one implementation, the watchdog timer circuit includes a counter register that advances (e.g., incremented or decremented) with each clock. To prevent the watchdog timer circuit from becoming triggered, the watchdog timer circuit should be reset or reloaded by software. For example, the count register may be reset to a value to start the count over. If the count register is allowed to count to a final or maximum value, the watchdog timer circuit will become triggered, generating a triggered signal that causes the programmable logic integrated circuit to be reset. A reset causes a reloading of the configuration data used to program the programmable logic and embedded processor portions of the integrated data. The configuration data may be stored in an external nonvolatile storage memory.